
IN THE CLAIMS

A detailed listing of the pending claims is shown below. New claims 30-37 are added.

1. (Cancelled)
2. (Previously Amended) A capacitor comprising:
at least four conductive layers embedded in a dielectric; and
a plurality of vias coupling the at least four conductive layers to a plurality of connection sites, wherein the capacitor has a thickness of between about .5 millimeter and about 1 millimeter.
3. (Original) The capacitor of claim 2, wherein the capacitor has a capacitance of between about 20 and about 30 microfarads.
4. (Cancelled)
5. (Previously Amended) A capacitor comprising:
at least four conductive layers embedded in a dielectric; and
a plurality of vias coupling the at least four conductive layers to a plurality of connection sites, wherein the plurality of vias are plated through holes.

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6. (Original) A capacitor comprising:

a plurality of first conductive layers, each of the plurality of first conductive layers formed on a first dielectric sheet;

a plurality of second conductive layers, each of the plurality of second conductive layers formed on a second dielectric sheet, and the plurality of second conductive layers interlaced with the plurality of first conductive layers;

a pair of dielectric sheets, each of the pair of dielectric sheets having a thickness slightly greater than about 7 microns, for providing a pair of substantially rigid outer surfaces for the plurality of second conductive layers interlaced with the plurality of first conductive layers, each of the pair of substantially rigid outer surfaces having a plurality of connection sites operable for coupling the capacitor to a substrate using a controlled collapse chip connection (C4); and

a plurality of vias coupling the plurality of first conductive layers and the plurality of second conductive layers to at least two of the plurality of connection sites.

7. (Original) The capacitor of claim 6, wherein each of the plurality of first conductive layers is fabricated from a tungsten paste.

8. (Original) The capacitor of claim 6, wherein the number of surfaces is two.

9.-10. (Cancelled)

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11. (Currently Amended) A capacitor comprising:
a multilayered capacitor having a pair of substantially rigid outer surfaces; and
a plurality of pads located on the pair of substantially rigid outer surfaces wherein
at least two of the plurality of pads are capable of being coupled to a substrate using a
solder bump, wherein the multilayered capacitor includes a number of parallel conductive
layers and the number of pads are coupled to the number of parallel conductive layers
through vias and The capacitor of claim 10, wherein the number of conductive layers is
greater than about 50.
12. (Original) The capacitor of claim 11, wherein the number of pads is greater than about 4000.
- 13.-29. (Cancelled)
30. (New) The capacitor of claim 2, wherein at least one of the at least four conductive layers comprises platinum.
31. (New) The capacitor of claim 3, wherein each of the at least four conductive layers comprises palladium.
32. (New) The capacitor of claim 5, wherein each of the at least four conductive layers comprises tungsten.
33. (New) The capacitor of claim 5, wherein each of the at least four conductive layers comprises palladium.
34. (New) The capacitor of claim 11, wherein the dielectric includes at least two outer layers, each of the two outer layers having a thickness of about 7 microns.

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35. (New) The capacitor of claim 34, wherein each of the at least four conductive layers comprises tungsten.

36. (New) The capacitor of claim 12, wherein each of the at least four conductive layers comprises platinum.

37. (New) The capacitor of claim 36, wherein the dielectric includes at least two outer layers, each of the two outer layers having a thickness of about 7 microns.